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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/656,791	09/08/2003	Kia Silverbrook	BAL52US	8951

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SILVERBROOK RESEARCH PTY LTD
393 DARLING STREET
BALMAIN, 2041
AUSTRALIA

EXAMINER	
MENBERU, BENIYAM	

ART UNIT	PAPER NUMBER
2625	

NOTIFICATION DATE	DELIVERY MODE
09/15/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/656,791	SILVERBROOK, KIA	
	Examiner	Art Unit	
	BENIYAM MENBERU	2625	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 August 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 7-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 7-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on *** has been entered.

Response to Arguments

2. Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over XP-002353310, "VLIW Processor Architecture Adapted to FPAs" to Petit et al in view of U.S. Patent Application Publication No. US 2001/0015760 A1 to Fellegara et al further

in view of U.S. Patent No. 4949189 to Ohmori further in view of U.S. Patent No. 5875034 to Shintani et al further in view of JP 06-103358 to Yamaki et al.

Regarding claim 1, Petit et al '310 discloses an image sensing and printing digital camera device (see Abstract) comprising:

an area image sensor positioned on the housing for sensing a viewed image (Figure 1, CMOS image sensor; Introduction second paragraph) and for generating pixel data representing the viewed image (see Introduction, seventh paragraph);

a one-chip microcontroller provided in the housing (Figure 1, shows one-chip microcontroller; see Abstract; Introduction first paragraph), the one-chip microcontroller integrating on the one chip a VLIW processor (Figure 1, shows VLIW processor integrated on the one-chip; Introduction sixth paragraph), an area image sensor interface connected to the VLIW processor (Figure 1, shows interface between CMOS sensor and ADC (analog to digital converter); Introduction seventh paragraph).

Petit et al '310 does not expressly disclose a printhead interface connected to the processor.

However, it is well known in the art to transfer image data for printing using the IEEE 1934 interface shown in Petit et al '310 in Figure 1.

Thus this interface can provide a printing interface for the one-chip disclosed in Petit et al '310.

It would have been obvious at the time the invention was made to one of ordinary skill in the art to provide Petit et al '310, with the well known ability to provide a printing interface.

However Petit et al '310 does not disclose:

a housing defining a slot for receiving a printed instruction card;

a linear image sensor for scanning the printed instruction card and converting into a data signal;

a linear image sensor interface ;

an input buffer connected to both the area image sensor interface and the linear image sensor interface, the input buffer receiving the pixel data and the data signal, the input buffer being further connected to the processor to effect communication of the pixel data and the data signal thereto.

Fellegara et al '760 discloses a housing defining a slot for receiving a printed instruction card (page 10, paragraph 73; "film chamber" 98 is housing/slot for receiving film cartridge; page 10, paragraph 74; the film cartridge has encoded data on the surface which can be optically encoded; this data reads on printed instruction; the surface of film cartridge reads on card.);

a linear image sensor for scanning the printed instruction card and converting into a data signal (page 10, paragraph 74; sensor 107 reads the encoded data and converts to identification code (data signal) for use by processor 120);

a linear image sensor interface (page 10, paragraph 74; Figure 6; unit 68 acts as interface between sensor 107 and the digital unit 72 (page 5, paragraph 46); the digital subsystem 72 acts as the one-chip controller having processor 120 and having interface with sensor 107 through unit 68);

input buffers connected to the area image sensor interface and the linear image sensor interface, the **input buffers** receiving the pixel data and the data signal, the **input buffers** being further connected to the processor to effect communication of the pixel data and the data signal thereto (pages 4-5, paragraph 44; page 10, paragraph 74; **data unit 122** provides the buffering of data (FIFO) from area image sensor unit in the analog system 70 (page 4, paragraph 41; CCD sensor 94 is the area image sensor); and **controller 68** acts as buffer of data coming from sensor 107 (linear image sensor) (page 10, paragraph 74); pages 4-5, paragraph 44; page 10, paragraph 74; data unit 122 provides communication between area sensor 94 of analog unit 70. The processor 120 of digital unit 72 receives pixel data from data unit 122 (buffer for area image sensor interface) and identification code (data signal) through controller 68 (buffer for linear image sensor interface).).

Having the system of ***Petit et al '310*** and then given the well-established teaching of ***Fellegara et al '760***, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the system of ***Petit et al '310*** as taught by ***Fellegara et al '760***, since ***Fellegara et al '760*** stated in page 10, paragraph 73, such a modification would provide identifiers to images in the form of tags.

However Petit et al '310 does not disclose an input buffer connected to both the area image sensor interface and the linear image sensor interface.

Ohmori '189 discloses an input buffer connected to both the area image sensor interface and the linear image sensor interface (Figure 1, switch 4 acts as buffer for line sensors 3a and 3b; column 3, lines 14-37).

Having the system of ***Petit et al '310*** and then given the well-established teaching of ***Ohmori '189***, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the system of ***Petit et al '310*** as taught by ***Ohmori '189***, since ***Ohmori '189*** stated in col. 1, lines 40-66, such a modification would provide efficient method to buffer data output from two sensors.

However Petit et al '310 does not disclose wherein the printed instruction card has printed thereon an array of dots representing a programming script and converting the array of dots into a data signal and the microcontroller decodes the data signal into the programming script and executes the programming script represented by the array of dots on the pixel data.

Yamaki et al '358 discloses wherein the printed instruction card has printed thereon an array of dots representing a programming script and converting the array of dots into a data signal and the microcontroller decodes the data signal into the programming script and executes the programming script represented by the array of dots on the pixel data (see Abstract; paragraph 2, 13, 15, 16; the data processing unit 5a is controlled to do image processing such as dithering, binarizing on image data based on the controller 8a which is programmed to determine the type of processing by analyzing the result of scanning the barcode (array of dots) on a paper (printed card).).

Having the system of ***Petit et al '310*** and then given the well-established teaching of ***Yamaki et al '358***, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the system of ***Petit et al '310*** as taught by ***Yamaki et al '358***, since ***Yamaki et al '358*** stated in Abstract section, such a

modification would provide the selection of different data processing based on the printed barcodes.

However Petit et al '310 does not disclose an image sensing and printing digital camera device and a printing mechanism arranged on the housing

Shintani et al '034 discloses an image sensing and printing digital camera device (Figure 1, CCD 101; column 7, lines 23-30; Figure 1, reference 111; column 7, lines 60-66); a printing mechanism arranged on the housing (column 6, lines 21-25; printer case; Figure 1 reference 111 is printer (column 7, lines 12-21;), and a printhead interface connected to the processor (Figure 1 shows interface between processor 102 and printer 111; Figure 5 shows print head unit 400, 403, 410; column 13, lines 63-67; column 14, lines 1-6;).

Having the system of ***Petit et al '310*** and then given the well-established teaching of ***Shintani et al '034***, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the system of ***Petit et al '310*** as taught by ***Shintani et al '034***, since ***Shintani et al '034*** stated in col. 3, Lines 55-67; column 4, lines 1-2, such a modification would provide a camera with embedded printer for providing user specified mode of printing.

Regarding claim 2, Petit et al '310 in view of Fellegara et al '760 further in view of Ohmori '189 further in view of Shintani et al '034 further in view of Yamaki et al '358 teaches all the limitations of claim 1. Further Shintani et al '034 discloses a device as

claimed in claim 1, wherein the area image sensor is one of a charge coupled device and an active pixel sensor (Figure 1, CCD 101; column 7, lines 23-30).

Regarding claim 3, Petit et al '310 in view of Fellegara et al '760 further in view of Ohmori '189 further in view of Shintani et al '034 further in view of Yamaki et al '358 teaches all the limitations of claim 1. Further Shintani et al '034 discloses a device as claimed in claim 1, wherein the printing mechanism includes an ink distribution assembly that is mounted on the print head assembly to distribute ink to the print head chips (column 18, lines 1-9, head 410 is pressed onto ink ribbon).

5. Claims 7, 8, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over XP-002353310, "VLIW Processor Architecture Adapted to FPAs" to Petit et al in view of U.S. Patent Application Publication No. US 2001/0015760 A1 to Fellegara et al further in view of U.S. Patent No. 4949189 to Ohmori further in view of U.S. Patent No. 5875034 to Shintani et al further in view of JP 06-103358 to Yamaki et al further in view of U.S. Patent No. 6070805 to Kaufman et al.

Regarding claim 7, Petit et al '310 in view of Fellegara et al '760 further in view of Ohmori '189 further in view of Shintani et al '034 further in view of Yamaki et al '358 teaches all the limitations of claim 1. Further Yamaki et al '358 discloses a device as claimed in claim 1, wherein the linear image sensor is an optical reader (see Abstract: barcode sensor 11a). However Yamaki et al '358 does not disclose wherein the array of dots is a two-dimensional array.

Kaufman et al '805 discloses wherein the array of dots is a two-dimensional array (Figure 4; column 2, lines 46-60).

Having the system of ***Petit et al '310 in view of Fellegara et al '760 further in view of Ohmori '189 further in view of Shintani et al '034 further in view of Yamaki et al '358*** and then given the well-established teaching of ***Kaufman et al '805***, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the system of ***Petit et al '310 in view of Fellegara et al '760 further in view of Ohmori '189 further in view of Shintani et al '034 further in view of Yamaki et al '358*** as taught by ***Kaufman et al '805***, since ***Kaufman et al '805*** stated in col. 2, lines 61-67, such a modification would provide increase amount of information that can be stored in the array of dots.

Regarding claim 8, Petit et al '310 in view of Fellegara et al '760 further in view of Ohmori '189 further in view of Shintani et al '034 further in view of Yamaki et al '358 teaches all the limitations of claim 7. Further Petit et al '310 discloses the device as claimed in Claim 7, wherein the one-chip microcontroller includes a program memory (Figure 1, the one-chip has **instruction (program)** and data memory), and the one-chip microcontroller is operable to write the program script to the program memory (page 129, fourth paragraph; instructions are stored in instruction memory) and Shintani et al '034 discloses further operable to run the program script from the program memory to define a software algorithm by which registers in the printhead interface are addressed to apply a desired effect to the pixel data (processor 100 is programmed to execute processing (column 13, lines 16-20); Figure 1, processor 100 interfaces the printing

section 111; column 13, lines 1-15; "desired print system" on column 13, line 11; column 13, lines 16-20, 56-61; One desired effect is multi-image effect which can print multi-image. Column 19, lines 9-25; head unit contains registers 501, 502).

Regarding claim 10, Petit et al '310 in view of Fellegara et al '760 further in view of Ohmori '189 further in view of Shintani et al '034 further in view of Yamaki et al '358 further in view of Kaufman et al '805 teaches all the limitations of claim 8. Further Petit et al '310 discloses the device as claimed in claim 8, wherein the VLIW processor receives pixel data from the image sensor, converts the pixel data into an internal format, and writes the converted pixel data to the DRAM memory interface (Introduction: seventh and eighth paragraph; ADC converts to digital format for writing into register; Figure 1 shows data memory control unit which interfaces with SLDRAM; page 131 paragraph before "SIMULATION RESULTS" section.).

6. Claims 9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over XP-002353310, "VLIW Processor Architecture Adapted to FPAs" to Petit et al in view of U.S. Patent Application Publication No. US 2001/0015760 A1 to Fellegara et al further in view of U.S. Patent No. 4949189 to Ohmori further in view of U.S. Patent No. 5875034 to Shintani et al further in view of JP 06-103358 to Yamaki et al further in view of U.S. Patent No. 6094282 to Hoda et al.

Regarding claim 9, Petit et al '310 in view of Fellegara et al '760 further in view of Ohmori '189 further in view of Shintani et al '034 further in view of Yamaki et al '358 teaches all the limitations of claim 1. Petit et al '310 discloses a one-chip microcontroller

and a VLIW processor (Figure 1, shows one-chip microcontroller; see Abstract; Introduction first paragraph; Figure 1, shows VLIW processor integrated on the one-chip; Introduction sixth paragraph). However Petit et al '310 in view of Fellegara et al '760 further in view of Ohmori '189 further in view of Shintani et al '034 further in view of Yamaki et al '358 does not disclose the device as claimed in claim 1, further including an output buffer, the output buffer effecting communication between the processor and the printhead interface.

Hoda et al '282 discloses an output buffer, the output buffer effecting communication between the processor and the printhead interface (Figure 5 shows processor 415 in communication with memory 418 (output buffer) which is connected to printhead unit 419; column 8, lines 24-42, 61-67).

Having the system of ***Petit et al '310 in view of Fellegara et al '760 further in view of Ohmori '189 further in view of Shintani et al '034 further in view of Yamaki et al '358*** and then given the well-established teaching of ***Hoda et al '282***, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the system of ***Petit et al '310 in view of Fellegara et al '760 further in view of Ohmori '189 further in view of Shintani et al '034 further in view of Yamaki et al '358*** as taught by ***Hoda et al '282***, since ***Hoda et al '282*** stated in col. 8, lines 37-42, 61-67, such a modification would provide the buffering of a line of printing data for the printhead system.

Regarding claim 11, Petit et al '310 in view of Fellegara et al '760 further in view of Ohmori '189 further in view of Shintani et al '034 further in view of Yamaki et al '358

further in view of Hoda et al '282 teaches all the limitations of claim 9. Petit et al '310 discloses the VLIW processor (Figure 1, shows VLIW processor integrated on the one-chip; Introduction sixth paragraph). Further Hoda et al '282 discloses the device as claimed in claim 9, wherein the processor converts the pixel data to print image data, and writes the print image data to the output buffer (column 8, lines 20-34, 37-42; processor converts image data to print data using data from Table 417. the converted data is output to memory 418 (output buffer).).

Other Prior Art Cited

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 5719970 to Aoki et al discloses image processor.

U.S. Patent No. 5966553 to Nishitani et al discloses a camera.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BENIYAM MENBERU whose telephone number is (571) 272-7465. The examiner can normally be reached on 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Moore can be reached on (571) 272-7437. The fax phone number for the organization where this application or proceeding is assigned is **571-273-8300**.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the customer service office whose telephone number is (571) 272-2600. The group receptionist number for TC 2600 is (571) 272-2600.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see <http://pair-direct.uspto.gov/>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Examiner, Art Unit 2625

09/10/2009

/Mark K Zimmerman/

Supervisory Patent Examiner, Art Unit 2625